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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,914	09/27/2001	Sehat Sutardja	MP0115	5719

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EXAMINER
WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/966,914	Applicant(s) SUTARDJA	
	Examiner Alexander O Williams	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2002* .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *5,6,9,10,17,18,21 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,11-16,19,20,22-25,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Serial Number: 09/966914 Attorney's Docket #: MP0115

Filing Date: 9/27/01;

Applicant: Sutardja

Examiner: Alexander Williams

Applicant's election without traverse of Species I (figure 1 and claims 1-8, 11-20 and 22-28) in Paper No. 5, filed 7/12/02 is acknowledged. However, the restriction has been modified and claims that will be examiner are claims 1 to 4, 7, 8, 11 to 16, 19, 20, 22 to 25, 27 and 28.

This application contains claims 5, 6, 9, 10, 17, 18, 21 and 26 drawn to an invention non-elected without traverse in Paper No. 5.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the circuit board in claims 11 and 20, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Note: in claim 1, line 6, a semicolon ";" should be inserted after "chip."

Claims 3, 15 and 24 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, it is unclear and confusing to what is meant by "wherein the heat sink is substantially thermally isolated from the package substrate." It appears the heat sink is connected directly to the package substrate.

In claims 15 and 24, it is unclear and confusing to what is meant by "further including thermally isolating the heat sink from the package substrate." It appears the heat sink is connected directly to the package substrate.

Any of claims 3, 15 and 24 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 4, 7, 8, 11, 13 to 16, 19, 20, 22 to 25, 27 and 28, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Degani et al. (U.S. Patent # 6,282,100 B1) in view of Kobayashi et al. (U.S. Patent # 5,311,402).

For example, in claim 1, Degani et al. **(figure 3)** show an integrated chip package, comprising: at least one semiconductor chip **11** having a first surface and a second surface; an intermediate substrate **15** electrically coupled via conductive bumps **(not labeled, but shown between 11 and 15)** to the first surface of the least one semiconductor chip; a package substrate **21** having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires **25**; but fails to explicitly show a heat sink thermally coupled to the second surface of the semiconductor chip.

Kobayashi et al. is cited for showing a semiconductor device package having locating mechanism for properly positioning semiconductor device within the package. Specifically, Kobayashi et al. (figures 2 to 20) specifically **figure 2** discloses semiconductor chip **1** having a first surface and a second surface; an intermediate substrate **7** electrically coupled via conductive bumps **6** to the first surface of the least one semiconductor chip; a package substrate **2** having a first surface electrically coupled to the intermediate substrate; and a heat sink **9** thermally coupled to the second surface of the semiconductor chip for the purpose of providing a heat radiation surface to increase to degrade the cooling effect.

Therefore, it would have been obvious to one of ordinary skill in the art to use Kobayashi et al.'s heat sink connecting to the chip to modify Degani et al.'s package for the purpose of providing a heat radiation surface to increase to degrade the cooling effect.

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Degani et al. (U.S. Patent # 6,282,100 B1) in view of Kobayashi et al. (U.S. Patent # 5,311,402) and further in view of Degani et al. (U.S. Patent # 5,869,894).

The combination of Degani et al. and Kobayashi et al. show the features of the claimed invention detailed above, but fail to explicitly show a support material arranged between the package substrate and the intermediate substrate.

Degani et al. is cited for showing a RF IC package. Specifically, Degani et al. **(figures 2 and 3)** discloses a semiconductor chip **13** having a first surface and a second surface; an intermediate substrate **14** electrically coupled via conductive bumps **16** to the first surface of the least one semiconductor chip; a package substrate **19** having a first surface electrically coupled to the intermediate substrate; and a support material arranged between the package substrate and the intermediate substrate for the purpose of preventing chips noise problems that frequently arise due to interconnects that are long or ineffectively placed.

Therefore, it would have been obvious to one of ordinary skill in the art to use Degani et al.'s support material and Kobayashi et al.'s heat sink connecting to the chip to modify Degani et al.'s package for the purpose of preventing chips noise problems that frequently arise due to interconnects that are long or ineffectively placed.

Claims 1 to 4, 7, 8, 11 to 16, 19, 20, 22 to 25, 27 and 28, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Boyle et al. (U.S. Patent # 6,020,646) in view of Kobayashi et al. (U.S. Patent # 5,311,402).

For example, in claim 1, Boyle et al. **(figures 1, 3 and 4)** specifically figure 1 show an integrated chip package, comprising: at least one semiconductor chip **110** having a first surface and a second surface; an intermediate substrate **130** electrically coupled via conductive bumps **122** to the first surface of the least one semiconductor chip; a package substrate **150** having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires **142**; but fails to explicitly show a heat sink thermally coupled to the second surface of the semiconductor chip.

Kobayashi et al. is cited for showing a semiconductor device package having locating mechanism for properly positioning semiconductor device within the package. Specifically, Kobayashi et al. (figures 2 to 20) specifically **figure 2** discloses semiconductor chip **1** having a first surface and a second surface; an intermediate substrate **7** electrically coupled via conductive bumps **6** to the first surface of the least one semiconductor chip; a package substrate **2** having a first surface electrically coupled to the intermediate substrate; and a heat sink **9** thermally coupled to the second surface of the semiconductor chip for the purpose of providing a heat radiation surface to increase to degrade the cooling effect.

Therefore, it would have been obvious to one of ordinary skill in the art to use Kobayashi et al.'s heat sink connecting to the chip to modify Boyle et al.'s package for the purpose of providing a heat radiation surface to increase to degrade the cooling effect.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,778,737,738,734,712,704,710,717,720,532,724,728,725	7/26/02
Other Documentation: foreign patents and literature in 257/686,685,723,777,778,737,738,734,712,704,710,717,720,532,724,728,725	7/26/02
Electronic data base(s): U.S. Patents EAST	7/26/02

Papers related to this application may be submitted to Technology Cent r 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

7/28/02

Primary Examiner
Alexander O. Williams